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Terms	Documents
L3 and spacers	7

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Search: L4

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DATE: Saturday, September 25, 2004 Printable Copy Create Case

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DB=USPT; PLUR=YES; OP=ADJ			
L4	L3 and spacers	7	L4
L3	L1 and silicide	23	L3
L2	L1 and silicid	0	L2
L1	(semiconductor adj device) near5 fin	248	L1

END OF SEARCH HISTORY

Hit List

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Search Results - Record(s) 1 through 7 of 7 returned.

1. Document ID: US 6764884 B1

L4: Entry 1 of 7 File: USPT Jul 20, 2004

US-PAT-NO: 6764884
DOCUMENT-IDENTIFIER: US 6764884 B1

TITLE: Method for forming a gate in a FinFET device and thinning a fin in a channel region of the FinFET device

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw De

2. Document ID: US 6555433 B2

L4: Entry 2 of 7 File: USPT Apr 29, 2003

US-PAT-NO: 6555433
DOCUMENT-IDENTIFIER: US 6555433 B2

TITLE: Method of manufacture of a crown or stack capacitor with a monolithic fin structure made with a different oxide etching rate in hydrogen fluoride vapor

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw De

3. Document ID: US 6476437 B2

L4: Entry 3 of 7 File: USPT Nov 5, 2002

US-PAT-NO: 6476437
DOCUMENT-IDENTIFIER: US 6476437 B2

TITLE: Crown or stack capacitor with a monolithic fin structure

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw De

4. Document ID: US 6344392 B1

L4: Entry 4 of 7 File: USPT Feb 5, 2002

US-PAT-NO: 6344392
DOCUMENT-IDENTIFIER: US 6344392 B1

TITLE: Methods of manufacture of crown or stack capacitor with a monolithic fin structure made with a different oxide etching rate in hydrogen fluoride vapor

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw De

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☐ 5. Document ID: US 5966609 A

L4: Entry 5 of 7 File: USPT Oct 12, 1999

US-PAT-NO: 5966609
DOCUMENT-IDENTIFIER: US 5966609 A

TITLE: Method of fabricating dome-shaped semiconductor device

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw De

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☐ 6. Document ID: US 5411912 A

L4: Entry 6 of 7 File: USPT May 2, 1995

US-PAT-NO: 5411912
DOCUMENT-IDENTIFIER: US 5411912 A

TITLE: Method of making a semiconductor device comprising lower and upper silicon layers as capacitor electrodes

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw De

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☐ 7. Document ID: US 5336922 A

L4: Entry 7 of 7 File: USPT Aug 9, 1994

US-PAT-NO: 5336922
DOCUMENT-IDENTIFIER: US 5336922 A

TITLE: Device comprising lower and upper silicon layers as capacitor electrodes and method of manufacturing such devices

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw De

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Terms	Documents
L3 and spacers	7

Display Format: TI Change Format

Previous Page Next Page Go to Doc#

L4: Entry 1 of 7 File: USPT Jul 20, 2004

DOCUMENT-IDENTIFIER: US 6764884 B1
TITLE: Method for forming a gate in a FinFET device and thinning a fin in a channel region of the FinFET device

Brief Summary Text (10):
According to the present invention, the foregoing and other advantages are achieved in part by a method of forming a gate in a FinFET device. The method includes depositing a first dielectric layer over a silicon on insulator (SOI) wafer, where the SOI wafer includes a silicon layer on an insulating layer. The method also includes forming a resist mask over a portion of the first dielectric layer, etching portions of the first dielectric layer and silicon layer not covered by the resist mask to form a fin and a dielectric cap covering a top surface of the fin. The method further includes depositing a gate layer over the dielectric cap, depositing a second dielectric layer over the gate layer, etching the gate layer and second dielectric layer to form a gate structure, forming sidewall spacers adjacent the gate structure and forming a third dielectric layer over the gate structure and sidewall spacers. The method also includes planarizing the third dielectric layer to expose a top surface of the second dielectric layer, removing the second dielectric layer and the gate layer in the gate structure, etching the fin to reduce a width of the fin in a channel region of the semiconductor device and depositing a gate material to replace the removed gate layer.

Brief Summary Text (11):
According to another aspect of the invention, a method of manufacturing a semiconductor device is provided. The method includes forming a fin structure on an insulating layer, where the fin structure includes a conductive fin. The method also includes forming source and drain regions, forming a gate over the fin structure and removing the gate to create a recessed area. The method further includes thinning a width of the fin in a channel region of the semiconductor device and depositing a metal in the recessed area.

Drawing Description Text (8):
FIG. 4 is a cross-section illustrating the formation of sidewall spacers adjacent the gate structure in accordance with an exemplary embodiment of the present invention.

Drawing Description Text (9):
FIGS. 5A and 5B are cross-sections illustrating the formation of metal-silicide compound on the device of FIG. 4 in accordance with an exemplary embodiment of the invention.

Detailed Description Text (11):
A dielectric layer may then be deposited and etched to form spacers 410 adjacent opposite sides of dummy gate 300, as illustrated in FIG. 4. Spacers 410 may comprise a silicon oxide (e.g., SiO.sub.2) or another dielectric material. In an exemplary implementation, the width of spacers 410 may range from about 50 .ANG. to about 1000 .ANG.. Spacers 410 may protect underlying fin 210 during subsequent processing and facilitate doping of source/drain regions 220 and 230.

Detailed Description Text (12):

A metal layer 510 may be deposited over source/drain regions 220 and 230, as illustrated in FIG. 5A. In an exemplary implementation, metal layer 510 may include nickel, cobalt or another metal, and may be deposited to a thickness ranging from about 50 .ANG. to about 200 .ANG.. A thermal annealing may then be performed to form a metal-silicide layer 520, as illustrated in FIG. 5B. During the annealing, the metal may react with the silicon in source/drain regions 220 and 230 to form a metal-silicide compound, such as NiSi or CoSi.sub.2, based on the particular metal layer 510 deposited.

Detailed Description Text (13):
Next, a dielectric layer 610 may be deposited over semiconductor device 100. In an exemplary implementation, dielectric layer 610 may include a tetraethyl orthosilicate (TEOS) compound and may be deposited to a thickness ranging from about 2000 .ANG. to 3000 .ANG.. In alternative implementations, other dielectric materials may be used. The dielectric layer 610 may then be planarized. For example, a chemical-mechanical polishing (CMP) may be performed to planarize the dielectric layer 610 with the upper surface of dielectric cap 320 and to expose the upper surface of dielectric cap 320, as illustrated in FIG. 7A. The dielectric cap 320 may then be removed using, for example, a wet etching procedure, as illustrated in FIG. 7B. In an exemplary implementation, the wet etch may use an acid, such as H.sub.3 PO.sub.4, to remove dielectric cap 320. During the etching process to remove dielectric cap 320, an upper portion of spacers 410 and dielectric layer 610 may also removed such that the upper surface of silicon layer 310 is substantially planar with the upper surface of spacers 410 and dielectric layer 610, as illustrated in FIG. 7B.

Detailed Description Text (14):
Silicon layer 310 may then be removed, as illustrated in FIG. 8. For example, silicon layer 310 may be etched using reactants that have a high etch selectivity with respect to polysilicon. This enables silicon material 310 to be removed without removing significant portions of any of the surrounding dielectric layers, such as spacers 410 and dielectric layer 140. After silicon layer 310 is removed, a gate opening or recess 810 is formed, as illustrated in FIG. 8. In other words, a gate-shaped space, referred to as gate recess 810, may be created in surrounding dielectric layer 610.

Detailed Description Text (15):
After the gate recess 810 is formed, the side surfaces of silicon fin may be exposed in the channel region of semiconductor device 100. Fin 210 may then be etched to reduce the width of fin 210 in the channel region. For example, a wet etch process may be performed to reduce the width of fin 210 in the channel region. Portions of fin 210 not in the channel region and source/drain regions 220 and 230 are covered by dielectric layer 610, which prevents those portions of semiconductor device 100 from being etched while the desired portion of fin 210 is thinned.

Detailed Description Text (16):
FIG. 9 illustrates a top view of semiconductor device 100 after the etching. Referring to FIG. 9, the dotted lines illustrate the thinned portion of fin 210 in the channel region. In an exemplary implementation, the overall width of fin 210 may be reduced by about 20 nanometers (nm) to 100 nm as a result of the etching. The width of fin 210 in the channel region after the etching, labeled as W in FIG. 9, may range from about 30 .ANG. to about 500 .ANG., in an exemplary implementation of the present invention. It should be understood that the width of fin 210 may depend on the particular device requirements and other parameters, such as the gate length. Area 810 in FIG. 9 illustrates the gate recess after removal of the dummy gate 300. The dielectric layer 610 and sidewall spacers 410 are not shown in FIG. 9 for simplicity.

Detailed Description Text (17):
Advantageously, thinning the width of fin 210 in the channel region enables the

L4: Entry 2 of 7 File: USPT Apr 29, 2003

DOCUMENT-IDENTIFIER: US 6555433 B2
TITLE: Method of manufacture of a crown or stack capacitor with a monolithic fin structure made with a different oxide etching rate in hydrogen fluoride vapor

Brief Summary Text (8):
U.S. Pat. No. 5,631,184 of Ikemasu et al. describes a "Method of Producing a Semiconductor Device Having a Fin-type Capacitor."

Detailed Description Text (3):
The stacks 21A-21D include gate oxide regions GOX on which polysilicon conductor/gate electrode layers 16 are formed on the surface of substrate 12. On each of the polysilicon conductor/gate electrode layers 16 is a refractory metal silicide layer 19 such as tungsten silicide (WSi.sub.2), a cap layer usually composed of silicon dioxide (SiO.sub.2) layer 20 and a silicon nitride (Si.sub.3 N.sub.4) layer 22 which can be implemented, as is well understood by those skilled in the art and as is described in the U.S. Pat. No. 5,792,689 of Fu-Lian Yang and Erik S. Jeng for "Method for Manufacturing Double Crown Capacitors Self-Aligned to Node Contacts on Dynamic Random Access".

Detailed Description Text (4):
Silicon dioxide sidewall spacers SP are formed on the sidewalls of the layers 16, 19, 20 and 22 of stacks 21A-21D as described in Liaw et al U.S. Pat. No. 5,712,202. Layers 20, 22 and spacers SP insulate the layers 16/19 from the polysilicon plugs PL which are formed between stacks 21A/21B and 21C/21D which reach the capacitor node contacts where plugs PL are formed on the surface of P-substrate 12.

Detailed Description Text (6):
A planarizing insulating layer 24 composed of BPSG has been formed as described in Liaw et al U.S. Pat. No. 5,712,202 covering the stacks 21A-21D and the substrate 12, but capacitor node contact openings have been formed between the sidewall spacers SP of stacks 21A and 21B on the left and between the sidewall spacers SP of stacks 21C and 21D on the right and those openings have been filled with metal, conductive plugs PL1/PL2 extending from contact with the N+ doped regions 14/14' respectfully on the surface of the substrate 12 between the stacks 21A/21B and between the stacks 21C/21D to the top surface of the BPSG layer 24.

CLAIMS:

7. A process comprising steps in the sequence as follows: forming a sublayer of a conductor layer in contact with a plurality of conductive plugs formed in a planarizing glass insulating layer which covers gate electrode/conductor stacks with spacers, with the conductive plugs in direct contact with the spacers, by the sequence as follows: forming a stack of silicon dioxide layers which are alternatingly doped and undoped on the conductive sublayer with the stack comprising a bottom layer formed on top of the conductive sublayer and each additional layer in the stack formed on a previous one of the layers in the stack including an undoped top silicon dioxide layer on top of the stack, with the doped silicon dioxide layers comprising BPSG layers, forming a mask over the stack with mask openings therethrough, etching the silicon dioxide layers through the mask openings to form capacitor-core-shaping cavities in the stack of silicon dioxide

layers reaching down through the stack to the conductive sublayer at the bottom of the stack, differentially etching the silicon dioxide layers in the cavities with a combination of hydrogen fluoride vapor and water vapor forming undercut edges in the doped silicon dioxide layers with the undoped silicon dioxide layers having cantilevered ribs projecting from the stack into the cavities to complete the plurality of molds, depositing a thick conductive layer into the cavities to form monolithic, solid capacitor cores with counterpart cantilevered ribs with a complementary pattern to the plurality of molds and the capacitor cores having inner cavities and a top surface, each of the monolithic, solid capacitor cores being formed of a material selected from the group consisting of aluminum, copper, tungsten, and titanium nitride and each of the monolithic, solid capacitor cores having a thickness from 500 .ANG. to 1,000 .ANG., polishing away the undoped top silicon dioxide layer of the plurality of molds and the top surface of each of the monolithic, solid capacitor cores by a Chemical Mechanical Planarization (CMP) process which removes the top undoped layer of the plurality of molds and the top of each of the monolithic, solid capacitor cores providing a flat upper surface thereof with a rib located on top of each of the monolithic, solid capacitor cores, etching away the plurality of molds, and then, after etching away the plurality of molds, etching back the sub layer to separate the thin, monolithic capacitor cores from adjacent thin, monolithic capacitor cores exposing the planarizing glass insulating layer.

Previous Doc Next Doc Go to Doc#